AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for achieving low gate leakage current in an integrated circuit during sleep mode, comprising reducing a power supply voltage applied to the integrated circuit to a low voltage level upon entering sleep mode, wherein the low voltage level is low enough to achieve low gate leakage current, but is high enough to maintain state in the integrated circuit, and wherein reducing the power supply voltage involves stepping the power supply voltage in discrete steps to the low voltage level to reduce noise caused by the voltage change.

2. (Original) The method of claim 1, wherein the low voltage level is so low that the integrated circuit cannot perform computation operations on data.

3. (Original) The method of claim 1, wherein the low voltage level is below a threshold voltage for transistors on the integrated circuit.

4. (Original) The method of claim 1, further comprising restoring the power supply voltage to a nominal operating voltage upon detecting that sleep mode is about to be exited.

5. (Original) The method of claim 4, wherein reducing the power supply voltage involves gradually ramping the power supply voltage to the low voltage level to reduce noise caused by the voltage change.

6. (Original) The method of claim 4, wherein restoring the power supply voltage involves gradually ramping the power supply voltage to the nominal operating voltage to reduce noise caused by the voltage change.

7 (Canceled).

8. (Original) The method of claim 4, wherein restoring the power supply voltage involves stepping the power supply voltage in discrete steps to the nominal operating voltage to reduce noise caused by the voltage change.

9. (Original) The method of claim 1, wherein the low voltage level is also low enough to provide a low subthreshold leakage current in the integrated circuit.

10. (Currently amended) An apparatus for achieving low gate leakage current in an integrated circuit during sleep mode, comprising a reducing mechanism configured to reduce a power supply voltage applied to the integrated circuit to a low voltage level upon entering sleep mode, wherein the low voltage level is low enough to achieve low gate leakage current, but is high enough to maintain state in the integrated circuit, and reducing the power supply voltage involves stepping the power supply voltage in discrete steps to the low voltage level to reduce noise caused by the voltage change.

11. (Original) The apparatus of claim 10, wherein the low voltage level is so low that the integrated circuit cannot perform computation operations on data.

12. (Original) The apparatus of claim 10, wherein the low voltage level is below a threshold voltage for transistors on the integrated circuit.

13. (Original) The apparatus of claim 10, further comprising a restoring mechanism configured to restore the power supply voltage to a nominal operating voltage upon detecting that sleep mode is about to be exited.

14. (Original) The apparatus of claim 13, wherein reducing the power supply voltage involves gradually ramping the power supply voltage to the low voltage level to reduce noise caused by the voltage change.

15. (Original) The apparatus of claim 13, wherein restoring the power supply voltage involves gradually ramping the power supply voltage to the nominal operating voltage to reduce noise caused by the voltage change.

16 (Canceled).

17. (Original) The apparatus of claim 13, wherein restoring the power supply voltage involves stepping the power supply voltage in discrete steps to the nominal operating voltage to reduce noise caused by the voltage change.

18. (Original) The apparatus of claim 10, wherein the low voltage level is also low enough to provide a low subthreshold leakage current in the integrated circuit.

19. (Currently amended) An integrated circuit that achieves low gate leakage current during sleep mode, comprising a reducing mechanism configured to reduce a power supply voltage applied to the integrated circuit to a low voltage

level upon entering sleep mode, wherein the low voltage level is low enough to achieve low gate leakage current, but is high enough to maintain state in the integrated circuit, and wherein reducing the power supply voltage involves stepping the power supply voltage in discrete steps to the low voltage level to reduce noise caused by the voltage change.

20. (Original) The integrated circuit of claim 19, wherein the low voltage level is so low that the integrated circuit cannot perform computation operations on data.

21. (Original) The integrated circuit of claim 19, wherein the low voltage level is below a threshold voltage for transistors on the integrated circuit.

22. (Original) The integrated circuit of claim 19, further comprising a restoring mechanism configured to restore the power supply voltage to a nominal operating voltage upon detecting that sleep mode is about to be exited.

23. (Original) The integrated circuit of claim 22, wherein reducing the power supply voltage involves gradually ramping the power supply voltage to the low voltage level to reduce noise caused by the voltage change.

24. (Original) The integrated circuit of claim 22, wherein restoring the power supply voltage involves gradually ramping the power supply voltage to the nominal operating voltage to reduce noise caused by the voltage change.

25 (Canceled).

26. (Original) The integrated circuit of claim 22, wherein restoring the power supply voltage involves stepping the power supply voltage in discrete steps to the nominal operating voltage to reduce noise caused by the voltage change.

27. (Original) The integrated circuit of claim 19, wherein the low voltage level is also low enough to provide a low subthreshold leakage current in the integrated circuit.